

# Benefits and Challenges in Decreasing GaAs Through Substrate Via Size and Die Thickness

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## ABSTRACT

**As the GaAs device market has shifted from primarily a low-volume military to a high-volume commercial customer base over the past decade, there has been significant pressure on manufacturers to reduce die and packaging costs. One obvious way to reduce die cost is to decrease the size enabling more die per wafer. Other important factors affecting cost include minimizing process cycle time, maximizing yield, and equipment utilization. The benefits and challenges in decreasing commercial GaAs device die size by reducing the through substrate via dimensions and die thickness will be presented. The impact of recent advances made in plasma etch and other equipment on this effort will be discussed.**

## INTRODUCTION

In order to meet the thermal conduction requirements of power GaAs MMICs (monolithic microwave integrated circuits) for military and satellite communication applications, small through substrate via sizes for 30-75  $\mu\text{m}$  thick wafers were developed over the past several years using reactive ion etch (RIE) tools.<sup>1-10</sup> This enabled through substrate ground vias to be located closer to the heat generating, active regions of power amplifier (PA) devices. For MESFET and pHEMT PAs, the vias were connected to the individual source fingers. Decreasing the standard die target thickness from 100  $\mu\text{m}$  to 75  $\mu\text{m}$  or less also enabled the back-side ground, plated heat sink to be placed closer to the device active regions resulting in better thermal conduction.

When GaAs wafers were thinned to a 75  $\mu\text{m}$  or less target thickness, two problems had to be overcome. First, handling of the thin wafers from the wafer / carrier de-mount through dicing steps without significant breakage presented a difficult challenge, especially for thin wafers that were diced into large area die. Some manufacturers met this challenge by plating a very thick layer of gold on the wafer back-side to serve as a grounded heat sink and provide mechanical support for the thin wafer.<sup>1, 2, 6, 7, 9</sup> Others developed a bathtub approach, which involved etching rectangular shaped tubs underneath the device active regions to enable even closer placement of the heat sink without compromising thin wafer / die handling.<sup>3, 5, 6,</sup>

<sup>11</sup> For small volume production serving military and

satellite communication applications, this approach proved successful. However for high volume commercial applications, such as base station and handset components, there was a trade-off involved with the extra steps needed to define and etch the bathtubs, which significantly added to the process cycle time and wafer fabrication cost. The second problem was that for high frequency power (X-band and higher) devices, a tight thickness tolerance was required in order to minimize variation in microstrip parameter values, which are a function of die thickness.<sup>7, 12, 13</sup> Also, the via inductance depends on the shape, height, and aspect ratio of the structure and must be accounted for in designs.<sup>14</sup>

The small via technology originally developed for high power, high frequency GaAs PAs for military and satellite communication applications can be utilized to lower the cost of commercial MESFET, HBT and pHEMT PA chips targeted for handset and Very Small Antenna Terminal (VSAT) applications. These chips can be used for applications ranging from the 900 MHz to the Ku frequency band. Since they tend to operate at lower frequencies than chips for military applications, the front-side of these die can often utilize low k dielectric BCB<sup>15-17</sup> or polyimide<sup>18, 19</sup> for the layers between the interconnect metal and for scratch protection of the finished circuitry. For the higher frequency bands, device designers need to carefully model the dielectric effects of BCB or polyimide into their circuits. These front-side polymer dielectric layers along with the back-side plated gold ground plane can provide the additional support needed for wafers thinned to 75  $\mu\text{m}$  or less in order to prevent breakage from the thin wafer / carrier de-mount through the dicing steps. The additional support can also enable the robust pick & place of very thin die from a UV (Ultra-Violet) dicing tape frame. The scratch protection provided by the polymer allows for robust placement into plastic packages, which are much less expensive than their ceramic counterparts. Most plastic packaged GaAs die are attached with thermal conductive epoxy in order to mitigate thermal mismatch issues and lower costs. Some PA die that generate a lot of excess heat may still need to be Au-Sn eutectic solder attached onto ceramic packages or module carriers.<sup>7, 20</sup>

There have been several recent published reports on using flip chip technology for GaAs MMICs.<sup>21-25</sup> Flip chip is an alternative technology to through substrate vias.<sup>2</sup> However, flip chip has been slow to gain wide acceptance

with GaAs devices. One reason for this may be the capital outlay required for new equipment needed for wafer bumping and flip chip die bonding to modules or boards. Flip chip wafer bumping foundries have recently started to solicit business from GaAs device manufacturers.

GaAs wafer thinning by using grinding followed by a spray wet etch or polish has been adopted in favor of mechanical lapping in order to meet high volume requirements.<sup>12, 20, 26, 27</sup> The older single spindle, multi-wafer grinding systems can easily achieve a  $100\pm 10$   $\mu\text{m}$  target thickness. However, better than a  $50\pm 5$   $\mu\text{m}$  target thickness is difficult.<sup>13</sup> Many 150 mm GaAs wafer Fabs have adopted single wafer, dual spindle automated wafer grinders with real time thickness monitoring to provide precise thickness control. To remove the grinding damage, some vendors offer a polish or spray etch module with their automated grinding systems. One vendor recently introduced an automated, contact-less wafer thickness measurement tool with an accuracy of less than  $\pm 0.5$   $\mu\text{m}$  and mapping capability.<sup>28</sup>

For 100 mm diameter GaAs wafer facilities, load-locked, four wafer per chamber RIE systems using  $\text{BCl}_3/\text{Cl}_2$  based chemistries have been used to etch small, through substrate vias with an average etch rate in the 0.3 to 0.35  $\mu\text{m}/\text{min}$  range.<sup>4, 9</sup> In these facilities via etch tends to be one of the major bottlenecks. Assuming a wafer target thickness of 50  $\mu\text{m}$  with 80% uptime and 80% utilization around the clock, each RIE chamber is capable of supporting only 170 wafers per week. For 150 mm facilities single wafer, cluster, inductively coupled plasma (ICP) systems have recently become the tool of choice.<sup>29</sup> Assuming similar uptime and utilization but an average etch rate of 2.5  $\mu\text{m}/\text{min}$ <sup>30</sup>, each ICP chamber is capable of supporting 320 150 mm wafers per week. For 100 mm facilities that plan to go to 150 mm in the near future, new ICP via etch systems can potentially alleviate a bottleneck situation.

The plasma ion density and bias voltage cannot be independently controlled in RIE chambers, so the maximum achievable etch rate for via etching is limited. ICP, ECR (electron cyclotron resonance), and dual frequency chambers offer an additional degree of freedom, which allows for independent control of the plasma ion density and bias. This enables average via etch rates for these tools to be several times higher than for RIE. At one time ECR was investigated for the small via etching application.<sup>31-33</sup> However, ICP has become the technology of choice for large scale production through substrate via etching largely owing to its ease of integration into a cluster tool format.<sup>29</sup> Also compared to ICP, ECR does not scale up as easily for larger wafer diameters, and its microwave power sources tend to be relatively unstable.<sup>34</sup>

Electroless plating can be used to deposit conformal seed layers into small, high aspect ratio vias. It has been used successfully for low-volume production.<sup>27, 35</sup>

However as volumes increased, most facilities adopted sputter systems for the seed layer deposition. As the via sizes decreased and aspect ratios increased, adequate sputtered seed layer coverage throughout the vias became a concern. This was addressed by tapering the shape of the vias to allow for more uniform coverage of the sidewalls and increasing the sputtered layer thickness to ensure a sheet resistance of less than 0.5  $\Omega/\text{sq}$  near the front-side metal pad. Also, long throw or collimated sputtering can be used to achieve improved seed layer coverage within high aspect ratio vias.<sup>36, 37</sup> In order to achieve more conformal coverage of the thick gold layer inside the vias, pulse has often been adopted versus DC plating since it offers better throwing power without sacrificing plating rate.<sup>20, 38</sup>

A tapered via profile is desirable if a solder-stop is required. For high-power PA die that require Au-Sn eutectic solder die attach onto ceramic packages or modules, a solder-stop metal is needed to prevent solder from flowing inside the vias.<sup>20, 27, 35</sup> Solder-stop metal can be blanket deposited over the plated gold on the back-side surface and inside the vias by sputter, electroplate, or electroless deposition. In order to remove the solder-stop metal from the back-side surface, a high-viscosity photoresist is typically used to cover the via to protect the solder-stop metal inside. For large vias the resist can be easily flowed into the holes using a programmable, multi-step dispense track. As the back-side surface via opening dimensions are reduced, it becomes increasingly difficult to reliably draw the resist into the holes, so a wetting agent is typically employed to alleviate this effect. Electrophoretic resist (EPR), which has been used successfully for conformal masking through vias in printed circuit boards<sup>39</sup>, is another option worth exploring. EPR has also recently been used for conformal masking applications on flat panel displays and high topography optical components.

An automated, thinned wafer de-mount tool equipped with a special thinned wafer robotic handling system that employs the Bernoulli effect has recently become available.<sup>40</sup> This tool uses two heated vacuum chucks that carefully clamp the thinned wafer and non-perforated carrier. The tool has successfully been demonstrated to work with the following temporary bonding adhesives: wax, liquid spin-on thermoplastic, dry film thermoplastic, and Nitto-Denko's new Revalpha heat release tape.

Dicing of 75  $\mu\text{m}$  or less thinned wafers usually requires the use of UV dice tape.<sup>41, 42</sup> Vendors recommend that the UV tape be exposed within 24 hours after the wafer is mounted on a tape frame in order to reduce the likelihood of residue adhesive remaining on the die back-side following pick & place.<sup>41-43</sup> Also, the UV tape should not be exposed to temperatures much higher than room temperature range for more than several minutes. Failure to follow these guidelines can result in organic residue being left on the die back-metal surface and the potential

for subsequent die attach issues. Upon UV exposure the adhesive strength of the tape decreases between one and two orders of magnitude enabling the thin, fragile die to be pick & placed from the dice tape.<sup>41-43</sup>

For high-power requiring eutectic solder attachment, a smaller die size is desirable in order to achieve a void-free die attach process if a “hot gas” die bonder platform is used.<sup>44</sup> A void-free attach process is needed to ensure reliable operation of power amplifier components.<sup>2, 44, 45</sup>

EXPERIMENTAL & DISCUSSION

The via dimension and die thickness reduction work was performed using a 100 mm diameter wafer equipment set, which included a batch wafer / carrier mount system, a batch / single spindle wafer grinder, a batch wafer polisher, an air pressure contact-less thickness gauge, two batch RIE systems with load-locks, a photoresist track, a barrel asher, and manual hotplates for de-mount. A spin-on thermoplastic adhesive was used for mounting the GaAs wafers onto slightly over-sized, non-perforated sapphire carriers.<sup>46</sup> The temporary wafer / carrier bond was performed in a batch Sharon Vacuum system equipped with spring loaded pressure plates, a programmable heating element, and a mechanical pump.

Table 1: Comparison of the two M/A-COM standard via sizes to the new via size for 2 mil thick die. MP90 is an HMDS based primer made by Shin-Etsu Chemical. Prop. means proprietary. \*If the 2 mil die can be successfully scribed instead of sawn then the dicing width can be reduced to 30 μm.

Front-side pad dimension (μm)	100	75	40
Die target thickness (μm)	100	100	50
8 μm BCB protection layer?	No	Yes	Yes
Photoresist mask opening (μm)	35	35	15
Back-side via opening (μm)	110	90	50
Front-side via opening (μm)	65	50	25
Wetting agent dispensed before photoresist	MP90	MP90	Prop.
125°C oven photoresist bake?	No	Yes	Yes
RIE via recipe (BCl <sub>3</sub> /Cl <sub>2</sub> )	1 step	2 step	2 step
Total etch time (min)	145	130	130
Average etch rate (μm/min)	0.69	0.77	0.38
Heated resist stripper for via mask?	No	Yes	Yes
Dicing street width (μm)	60	60	30*
Solder-stop flood expose/ develop process?	Yes	Yes	Yes

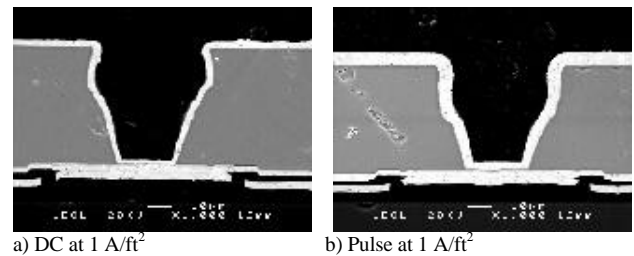
Several 100 mm GaAs HBT wafers coated with an 8 μm thick BCB scratch protection layer were successfully thinned to a 50±7 μm GaAs target thickness using the batch G&N 400 wafer grinder, Speedfam polisher, and Ames contact-less air pressure gauge. The total thickness variation (TTV) of less than or equal to 5 μm across the thinned wafers was primarily due to the spin-on thermoplastic mounting adhesive, the sapphire carrier, and the batch grinder.<sup>20, 46</sup> Polishing was used to remove the post grind damage since it tends to maintain a tighter TTV across the wafer than spray etching.

A two-step RIE etch process was developed in the batch Plasma Therm SLR720 load-locked system using a

BCl<sub>3</sub>/Cl<sub>2</sub> chemistry to obtain vase shape vias and the desired dimensions at the front-side metal pad boundary.<sup>10</sup> A comparison of this new small via size to M/A-COM standard via sizes is shown in Table 1. Adopting slot instead of vase via shapes may result in a slightly higher etch rate and throughput.<sup>4,9</sup>

Conformal back-side seed layer deposition was achieved on half the wafer lot by utilizing electroless Pd and Ni deposition in single-wafer baths.<sup>35</sup> Magnetron sputtering of a 50 nm TiW / 200 nm Au seed layer was done for the other half of the wafer lot in an old batch MRC tool. DC and pulsed gold sulfite electroplating was performed in single-wafer baths. A comparison of GaAs HBT through substrate via cross sections that underwent direct current (DC) and pulse electroplating is shown in Figure 1. Note that front-side (FS) to back-side (BS) gold deposit thickness ratios, which is a measure of conformal coverage, for the DC and pulse plated vias are similar. This indicates that pulse plating does not result in improved deposit conformal coverage in the vias under these conditions. Another presentation at this conference will cover design of experiment results on DC vs. pulse gold electroplating for GaAs wafer through substrate vias.<sup>47</sup> For die to be gold-tin solder attached (half the wafer lot), a 0.1 μm electroless Ni solder-stop layer was deposited on top of the electroplated gold.

Figure 1: A comparison of two GaAs HBT through substrate via cross sections for wafers that underwent DC and pulse gold electroplating. A conformal seed layer was obtained by electroless Pd and Ni deposition. The shape of the cross section varies slightly with cleave direction.



Duty cycle on / off (ms)	I <sub>av</sub> (mA)	Time (min)	Au BS (μm)	Au FS (μm)	FS/BS
DC (a)	85	45	2.8	1.8	0.64
5 / 5 (b)	85	90	5.5	3.2	0.57

Duty cycle on / off (ms)	GaAs t (μm)	Via opening BS (μm)	Via opening FS (μm)
DC (a)	51	50	24
5 / 5 (b)	46	52	26

Back-side streets were defined using a positive photoresist mask and a potassium iodide / iodine gold etch solution. For half the wafer lot, a dilute ferric chloride solution was used to etch through the Ni in the streets. In order for the thick, positive photoresist to fill the small, vase shaped vias, a proprietary wetting agent was also required (see Table 1). The new via resist fill dispense

was developed on a programmable MTI resist track equipped with a robotic wafer handler, robotic dispense arm, spin chuck & static bowl, hotplate, and cool plate. For die to be solder attached, a flood expose and develop step was used to clear photoresist from the back-side surface, while leaving behind most of the resist inside the vias. The solder-stop nickel was etched in dilute ferric chloride from the back-side surface, while most of the nickel inside the vias was protected by the fill resist.

De-mounting and cleaning the 50  $\mu\text{m}$  thick HBT wafers using manual hot-plates and heated solvent baths were performed by experienced operators with no breakage within the experimental wafer lot. Cracking was not a problem at die separation and pick & place into die packs. UV dicing tape and a Disco saw with an electroformed nickel bonded diamond blade were used for die separation.<sup>48</sup> A scribe & break process on Dynatex tools is being developed, so that the dicing streets may be decreased from 60 to 30  $\mu\text{m}$ .<sup>48</sup> All wafers processed so far have passed the MIL-STD 883 die qualification tests including tape test for back-metal adhesion and die shear. Au-Sn eutectic solder and epoxy die attach evaluations of 2 mil thick die is planned.

#### SUMMARY

The benefits of decreasing GaAs die size by reducing substrate via dimensions and die thickness were presented. The process challenges and trade-offs to achieve this reduction have been discussed. The process technology and equipment exists in order to successfully transition this size reduction into high volume, low cost manufacturing.

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