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InP Processing Using an HBr High Density ICP Plasma

David Lishan[1], Jewon Lee[2], Grant Kim[3]

[1]Unaxis USA, 10050 16th St. North, St. Petersburg, FL 33716
Phone: 727 577 4999, e-mail:david.lishan@unaxis.com
[2]Dept. of Optical Engineering, Inje University, 607 O-Bang-Dong Kimhae City KyooungNam, S. Korea
[3]Vitesse Semiconductor Corp., 741 Calle Plano, Camarillo, CA 93012

ABSTRACT

This work explores using hydrogen bromide (HBr) to etch InP and InGaAs in a high density inductively coupled plasma system (ICP). Noncrystallographic etch rates of approximately 1100 Å/min with excellent surface morphology (RMS<2.5 nm) can be obtained using HBr at near room temperature with active substrate cooling. Similar etch rates can be observed at elevated etch temperatures (160ºC) that provide undercut profiles assisting self-aligned structures. The effects of ICP power, substrate bias, temperature, and pressure on etch rate, profiles, and surface morphology will be discussed in the context of device fabrication steps such as mesas and self-aligned structures.

INTRODUCTION

One of the primary technologies for high speed, low power digital technology utilizes the InP material system. This technology is moving into high volume manufacturing but still frequently relies on wet etching to fabricate many device structures (e.g. HBTs) due to the difficulties associated with dry etch chemistries. InP compounds have traditionally been difficult to dry etch as a result of low etch rates, preferential loss of material, and subsequently rough surfaces. Prevailing approaches with chlorine chemistry and methane/hydrogen chemistry are not without significant drawbacks. Chlorine chemistry requiring elevated temperatures approaching 160ºC or significant ion bombardment is used to obtain acceptable surface morphology. Elevated temperature and substantial ion flux stretch the selectivity limits of photoresist as an adequate etch mask and for inducing acceptable damage in sensitive materials. Using methane and hydrogen as etch gases is complicated by slow etch rates, indium enrichment and polymer formation. Thus, the search continues for a chemistry that encompasses the positive aspects of wet etching and incorporates the advantages of dry processing. The goals being control of profile, etch rate, and surface morphology.

Bromine-based chemistry has been considered as a candidate for dry etching indium containing materials since the reaction product vapor pressures, $InBr_x$ and PBr_x, are considered relatively low compared to the respective chlorides. Pearton *et. al.* reported using combinations of HBr and Ar, H_2 and CH_4 in an electron cyclotron resonance discharge to produce clean surfaces[1]. Other groups have also used HBr to etch In containing compounds in RIE systems[2]. This work uses HBr by itself in an ICP system with an rf biased substrate. We report etch selectivity using photoresist and tungsten-nitride (WN_x) masks and the profiles using these materials. The profiles and surface are expected to be compatible with device fabrication.

EXPERIMENTAL

Etch rates were determined using profilometer step heights from patterned pieces of the material of interest. Pieces were mounted with thermal conductive paste on a 100 mm GaAs wafer. Wafers were etched in a Unaxis SLR system consisting of an ICP chamber (operating at 2 MHz) and an additional RF bias (13.56 MHz) for the sample chuck. Backside flowing helium was used with an active clamping configuration. Surface morphology was measured using a atomic force microscope (AFM) and profiles with a scanning electron microscope (SEM).

RESULTS and DISCUSSION

InP, $In_{0.53}Ga_{0.47}As$, GaAs, photoresist, and WN_x were etched for 2 min periods with 500 W ICP power and several substrate bias powers using HBr at low pressure and room temperature. These etching results are presented in Figure 1 and show that as the In fraction increases, the etch rate

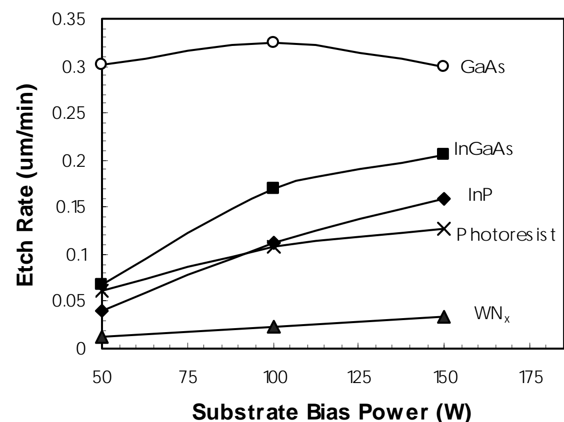


Figure 1. Effect of substrate bias power on 25ºC etch with HBr chemistry.

decreases. This is attributed to the relatively low volatility of the In products. In general, as the bias voltage increases with substrate bias power, the etching rate also increases. Selectivities based on etch rates with 100 W of substrate bias are shown in Table 1. Although substrate surface temperatures have likely exceeded the 25ºC setpoint of the substrate chuck, measurements under similar processing conditions indicate substrate temperatures less than 45ºC.

TABLE 1
Etch Selectivities to InP

Material	Selectivity
InP:InGaAs	~0.65
InP:PR	~1
InP:WN_x	~4

Figure 2 shows the etching rate as a function of ICP power. The decrease in etch rate is likely due to a reduction in the substrate bias voltage which drops from approximately 100 V over this ICP range.

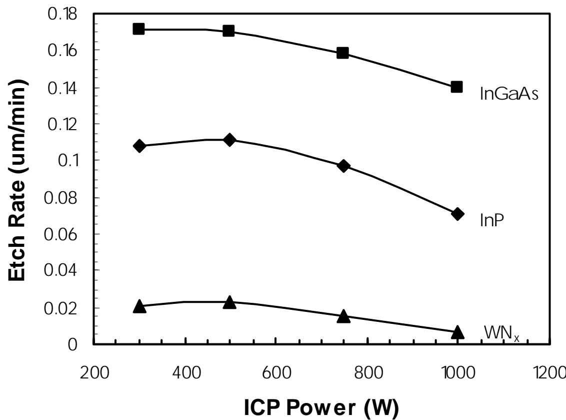


Figure 2. Etch rate as a function of ICP power.

The addition of Ar has the effect of reducing etch rates and increasing the surface roughness. The decrease in etch rate is again likely due to the decrease in bias voltage. For process conditions of 100 W substrate bias power and 500 W ICP the surface morphology was measured with an AFM. This data is provided in Table 2. The thin epitaxial layers used in compound semiconductor devices require that processing result in smooth surfaces.

TABLE 2
AFM Measured Surface Morphology

Process	Roughness (RMS)
unetched InP (as received)	0.4 nm
HBr	<2.5 nm
HBr/Ar	~5 nm
HBr/He	~4 nm

One of the drawbacks of wet etching is a correlation between pattern orientation to crystallographic directions and etch rate. The etching conditions used in this work indicate an absence of this behavior. A crossbar aligned along the 100 direction was etched and examined under a SEM. Figure 3 shows essentially no difference in feature width or shape in the orthogonal directions. More detailed measurements indicated the top or plateau portions of the etched features are equal in both directions.

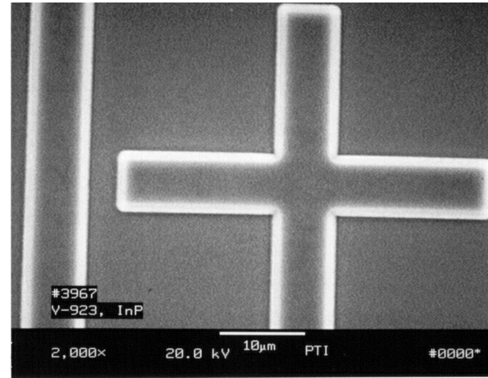


Figure 3. Top down SEM view of InP etched crossbar, with photoresist removed.

The profiles obtained with these room temperature etch conditions are positively sloped. This is to be expected with the selectivities shown in Table 1. Sidewall angle tends to be proportional to mask erosion (i.e. selectivity) and thus, the WN_x masked samples show more vertical features than photoresist samples, as the selectivity to WN_x is greater than photoresist. Figure 4 reveals SEM examples of this phenomenon.

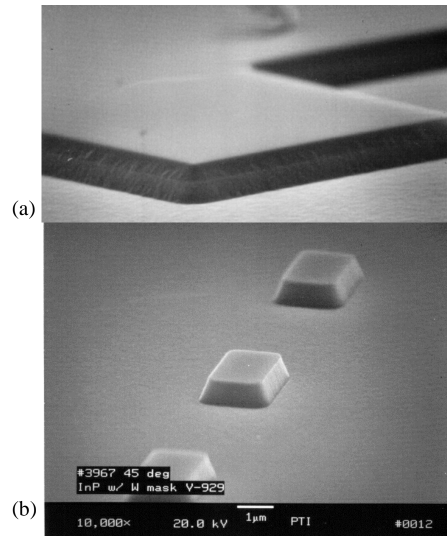


Figure 4. SEMs of InP etched features with photoresist (a) and (b) WN_x mask material still present.

Observation of higher and lower substrate bias conditions did not show a significant change in profile. However, the InP surface was clearly rougher for conditions of 50 W and 175 W. These profiles while not vertical may be suitable for mesas or emitter delineation.

Work was performed at elevated temperatures in attempts to obtain undercut profiles that might have utility for self-aligned type structures such as those found in HBT devices. Examples of profiles potentially useful for lift-off type processes are shown in Figure 5. The amount of undercut and the surface roughness are affected by the amount of substrate bias. In Figure 5, the lowest substrate bias power of 5 W produced the roughest surface while only a slight increase to 25 W of substrate bias produced a much smoother surface.

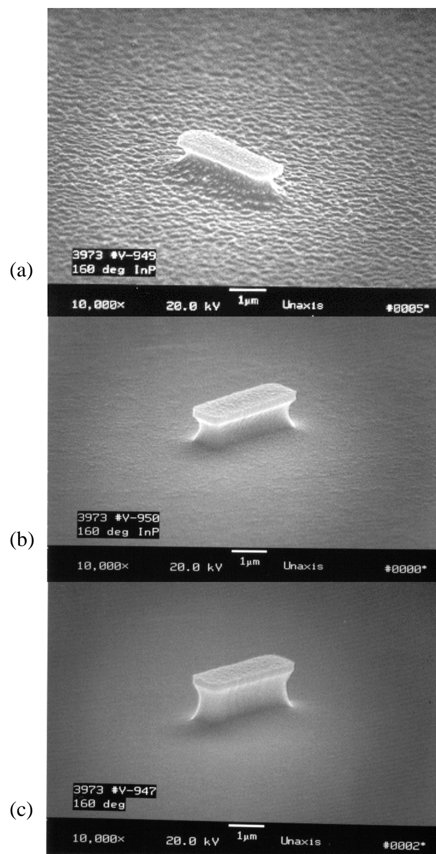


Figure 5. SEM of InP features using a W mask with increasing substrate bias power. a) 5 W, b) 15 W, c) 25 W.

An advantage of the low substrate bias levels is the high selectivity to the mask material. For example, WN_x etching was not detected at the substrate bias conditions of 25 W.

One of the challenges of etching at higher temperatures is maintaining controllable etch rates. Figure 6 shows the sensitivity of the process at 160ºC to low substrate bias and ICP powers.

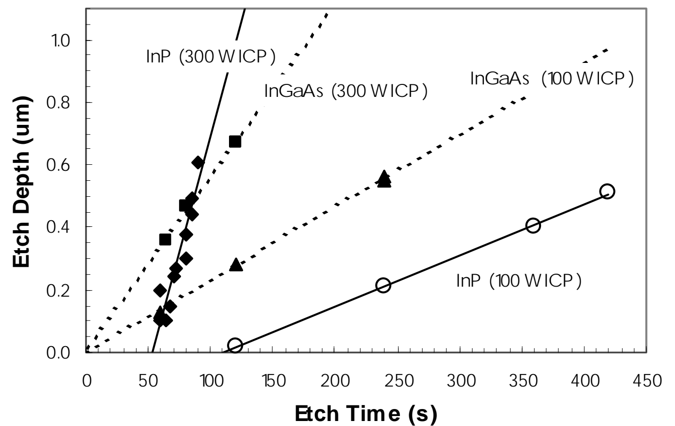


Figure 6. Etch depth as a function of etching time.

A study of etch rate versus substrate temperature indicates little change between 130ºC and 160ºC. However, the InP surface becomes rougher as the temperature is lowered.

As reported by others, the InP surface oxides can act as a weak etch mask. We believe etch induction times shown as the x-axis intercepts for the 100 W and 300 W ICP power data is evidence of this phenomenon. The absence of a delay in etching for InGaAs is suggestive but not conclusive that phosphorous oxides are the temporary impediment to etching. The InP etch rates as determined by the slope of the etch depth versus time plots are ~0.89 µm/min for the 300 W ICP condition and 0.1 µm/min for the 100 W process. Figure 6 shows differences in surfaces following etching for the two ICP levels.

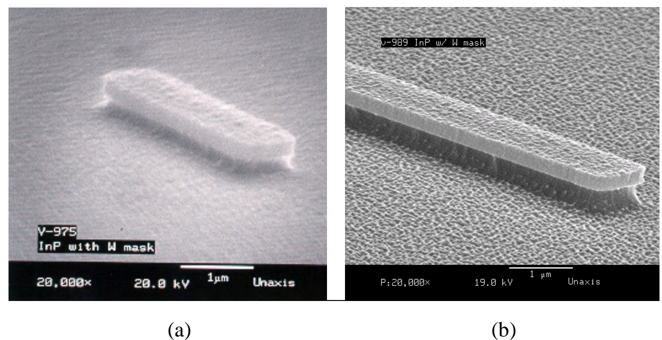
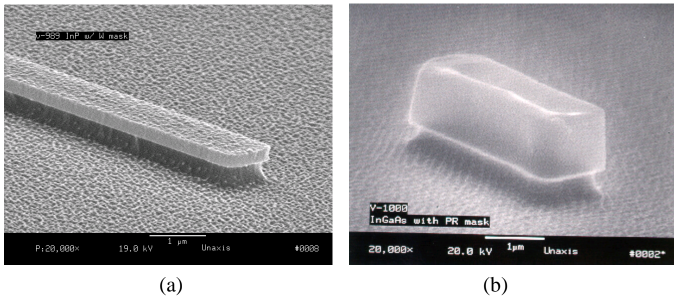


Figure 7. SEM of InP surface following etch. a) 300 W ICP, b) 100 W ICP.

For InGaAs the etching rates are 0.32 µm/min and 0.14 µm/min respectively. The difference in materials also generates a change in surface roughness. In Figure 8 it can be seen that the InGaAs material (with a photoresist mask) appears smoother than that for InP.



(a) (b)

Figure 8. SEM of a) InP, b) InGaAs surface following etch..

One would expect that oxidation of a "buried" InP layer would be avoided during growth of an epitaxial layer structure. Figure 9 shows the surface (via SEM) of an InP surface resulting after etching away a cap layer of InGaAs. The surface appears similar in roughness to that shown in Figure 7b. Surface roughness for the sample in Figure 9 is approximately 11 nm RMS as measured with AFM.

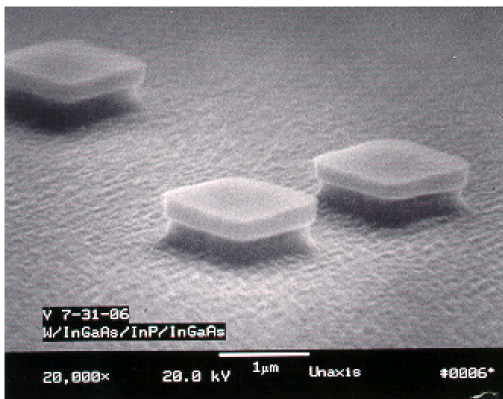


Figure 9. SEM photos of InP surface condition following etch of an InGaAs cap layer.

Successful etching of the thin layers comprising most epitaxial structures requires both a relatively slow etch rate and a means for controlling endpoint. The etching processes described thus far meet the criteria for a suitable rate. Monitoring the process can be accomplished with optical emission spectroscopy (OES). In Figure 10, OES data using a ratio of In and Ga line intensities (410 nm and 417 nm respectively) were recorded while etching at room temperature. Under the conditions used, no induction period prior to etching initiation was observed. The samples consisted of epitaxial InGaAs and InP layers and have been labeled in the figure with their intended function in an HBT device.

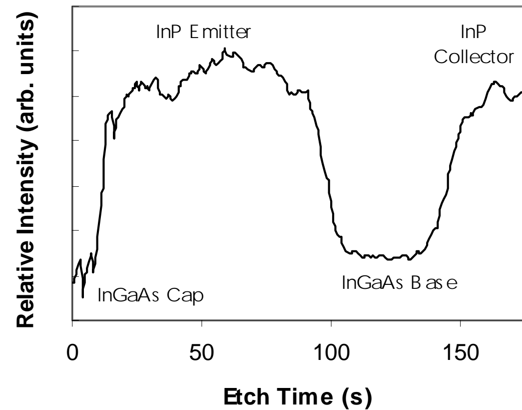


Figure 10. Optical emission intensity as a function of etch time for an epitaxial sample of InGaAs and InP.

CONCLUSION

HBr appears to be a suitable candidate for etching InP and InGaAs at either room temperature or elevated temperatures of approximately 160ºC. At room temperature smooth surfaces with surface roughness less than 2.5 nm RMS and a controllable, noncrystallographic etch rate of 0.11 µm/min is possible. Profiles are positively sloped using either photoresist or tungsten masks at ~45 and ~65 degrees slope respectively. These slopes may be appropriate for mesa or emitter features. Although etching with HBr at 160ºC with low substrate bias and ICP powers is primarily chemical in nature and not ion driven, crystallographic profiles are not observed. Low controllable etching rates of ~0.1 µm/min are achievable while maintaining useful surface morphology. Undercut profiles potentially suitable for self-aligned structures are generated.

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